IN THE CLAIMS

Please Amend the Claims in accordance with the following markup copy:

1. (Currently Amended) An interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits, said interface circuit comprising:

a node within said system controller integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits;

first switch means for selectively connecting said node to a first circuit of the system[[s]] controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit;

second switch means for selectively connecting said node to a second circuit of the system[[s]] controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit;

signal means for early enabling and late disabling of said first and second switch means consistent with setup and hold times of the respective first and second peripheral integrated circuits, and wherein said node is a bi-directional interface pin for interfacing bi-directional signals to said first peripheral integrated circuit, wherein first peripheral integrated circuit includes bi-directional input/output connections, wherein said

first switch means comprises a transmission gate having a select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said first circuit.

2. (Currently Amended) The interface circuit of Claim 1, wherein said node is further a bi-directional interface pin for interfacing bi-directional signals to said second peripheral integrated circuit and said second switch means comprises a transmission gate having a select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said second circuit ~~is an output pin for providing an output signal to said first one and said second one of said plurality of peripheral integrated circuits, and wherein said first switch means comprises a selector within said system controller integrated circuit having a select input coupled to signal means~~.

Claims 3-7 have been canceled.

8. (Currently Amended) ~~The interface circuit of Claim 7 further comprising:~~ An interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits, said interface circuit comprising:

a node within said system controller integrated circuit commonly connected to a first and a second one of said plurality

of peripheral integrated circuits;

first switch means for selectively connecting said node to a first circuit of the system controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit;

second switch means for selectively connecting said node to a second circuit of the system controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit;

signal means for early enabling and late disabling of said first and second switch means consistent with setup and hold times of the respective first and second peripheral integrated circuits;

first chip select signal means coupled to said first peripheral integrated circuit for enabling communication with said first peripheral integrated circuit; and

second chip select signal means coupled to said second peripheral integrated circuit for enabling communication with said second peripheral integrated circuit, and wherein said first switch means ~~circuit~~ comprises a first transparent latch having a gate input coupled to said first chip select signal means, whereby a state of said node may be maintained at said first peripheral integrated circuit when said first chip select signal[[s]] means deselects communication with said first peripheral integrated circuit~~, and wherein said second circuit~~

~~comprises a second transparent latch having a gate input coupled to said second chip select signal means, whereby a state of said node may be maintained at said second circuit when said signal means deselects said second peripheral integrated circuit~~.

9. (Currently Amended) The interface circuit of Claim 8 ~~1~~, wherein said node is a pin for receiving a first signal from said first peripheral integrated circuit and transmitting a second signal to said second peripheral integrated circuit, and wherein said second switch means comprises a tri-state buffer having an enable input coupled to said second chip select signal means and an ~~output~~ input coupled to said node and an ~~input~~ output coupled to said ~~first~~ second peripheral integrated circuit.

10. (Currently Amended) The interface circuit of Claim 8 [[9]], ~~wherein said first circuit comprises a transparent latch having a gate input coupled to said signal means, whereby a state of said node may be maintained when said signal means disables said gate input~~ wherein said second switch means comprises a second transparent latch having a gate input coupled to said second chip select signal means, whereby a state of said node may be maintained at said second circuit when said signal means deselects said second peripheral integrated circuit.

11. (Canceled).

12. (Currently Amended) A method for coupling a plurality of signals of differing types between a plurality of peripheral integrated circuits and a system controller integrated circuit, said method comprising:

generating a peripheral select signal within said system controller integrated circuit for early enabling and late disabling switch means consistent with setup and hold times of the peripheral integrated circuits;

generating a chip select signal from said peripheral select signal;

supplying said chip select signal to a corresponding peripheral integrated circuit chip select input;

selecting one of a plurality of internal signals each associated with one of said plurality of peripheral integrated circuits in conformity with said peripheral select signal; and

coupling said selected internal signal to an external pin connected to each of said plurality of peripheral integrated circuits, whereby said selecting and said coupling interfaces a internal signal associated with a peripheral integrated circuit corresponding to said chip select signal, and wherein said coupling provides bi-directional signal flow to and from said selected one of said plurality of internal signals and said external pin, whereby a bi-directional peripheral device pin can be interfaced to said selected internal signal.

13. (New) The method of Claim 12, wherein said selecting selects one of said plurality of internal signals at a time preceding said generating by a time greater than or equal to a maximum setup time among said first and second peripheral integrated circuits and continues to select said selected one of said plurality of internal signals until said generating is complete and a time greater than or equal to a maximum hold time among said first and second peripheral integrated circuits has elapsed.

14. (Canceled).

15. (Currently Amended) ~~The method of Claim 12, further comprising:~~ A method for coupling a plurality of signals of differing types between a plurality of peripheral integrated circuits and a system controller integrated circuit, said method comprising:

generating a peripheral select signal within said system controller integrated circuit for early enabling and late disabling switch means consistent with setup and hold times of the peripheral integrated circuits;

generating a chip select signal from said peripheral select signal;

supplying said chip select signal to a corresponding peripheral integrated circuit chip select input;

selecting one of a plurality of internal signals each associated with one of said plurality of peripheral integrated circuits in conformity with said peripheral select signal; and coupling said selected internal signal to an external pin connected to each of said plurality of peripheral integrated circuits, whereby said selecting and said coupling interfaces a internal signal associated with a peripheral integrated circuit corresponding to said chip select signal;

latching a signal value received from said external pin resulting from said coupling at an end of said generating; and

holding said signal value to maintain a state of one of said plurality of internal signals after an end of said coupling.

16. (Currently Amended) An interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits, said interface circuit comprising:

a node within said system controller integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits;

a selector for selectively connecting said node to one of a first circuit of the systems controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit and a second circuit of the systems controller integrated circuit for communicating signals with reference to

said second peripheral integrated circuit;

a chip select circuit providing a first chip select output for connection to a first chip select input of said first peripheral integrated circuit and a second chip select output for connection to a second chip select input of said second peripheral integrated circuit and an selection signal connected to said selector, wherein said selection signal is set to a state for selecting one of said first circuit and said second circuit at a time preceding assertion one of said chip select signals by a time greater than or equal to a maximum setup time among said first and second peripheral integrated circuits and is maintained in that state until said asserted one of said chip select signals is de-asserted and a time greater than or equal to a maximum hold time among said first and second peripheral integrated circuits has elapsed, and wherein said node is a bi-directional interface pin for interfacing a bi-directional signal to and from said first peripheral integrated circuit, wherein said first circuit includes a bi-directional input/output connection, and wherein said selector comprises a transmission gate having a select input coupled to said chip select circuit, a first terminal connected to said node and a second terminal coupled to said first circuit.

17. (Previously Submitted) The interface circuit of Claim 16, further comprising a transparent latch having an input coupled to an output of said selector, whereby a state of said node that

reflects an output of said selected one of said peripheral integrated circuits is held after said asserted one of said chip select signals is de-asserted.

Claims 18-19 have been Canceled.

20. (Currently Amended) The interface circuit of Claim 16[[9]], wherein said selector further comprises a second transmission gate having a select input coupled to said chip select circuit, a first terminal connected to said node and a second terminal coupled to a bi-directional signal of said second circuit.

21. (New) An interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits, said interface circuit comprising:

a node within said system controller integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits;

a selector for selectively connecting said node to one of a first circuit of the systems controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit and a second circuit of the systems controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit;

a chip select circuit providing a first chip select output for

connection to a first chip select input of said first peripheral integrated circuit and a second chip select output for connection to a second chip select input of said second peripheral integrated circuit and an selection signal connected to said selector, wherein said selection signal is set to a state for selecting one of said first circuit and said second circuit at a time preceding assertion one of said chip select signals by a time greater than or equal to a maximum setup time among said first and second peripheral integrated circuits and is maintained in that state until said asserted one of said chip select signals is de-asserted and a time greater than or equal to a maximum hold time among said first and second peripheral integrated circuits has elapsed; and

a transparent latch having an input coupled to an output of said selector, whereby a state of said node that reflects an output of said selected one of said peripheral integrated circuits is held after said asserted one of said chip select signals is de-asserted.